

ANDERSSON et al
Serial No. 09/829,451

Atty Dkt: 2380-187
Art Unit: 2665

AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 6, line 26, and continuing to page 7, line 6, as follows:

To certain switch ports of switch 32A which are outgoing from end node 22A are connected extension terminals 34A, only one such extension terminal 34A being shown in Fig. 1 for sake of simplification. Likewise, the outgoing switch ports of switch 32B are connected to extension terminals 34B. As is understood to those skilled in the art, ~~it~~ it is through extension terminals such as extension terminal 34A and extension terminal 34B that a switch 32 of a node in the physical layer is connected in the physical layer to other nodes. Various aspects of extension terminals (sometimes referred to as "exchange terminals") are described, e.g., in one or more of the following (all of which are incorporated herein by reference: United States Patent 6,128,295; United States Patent 6,088,359; United States Patent 5,963,553; United States Patent 6,154,459; and United States Patent 6,034,958. For example, each extension terminal 34 may be connected to one or more (e.g., four) cables or links to other nodes of telecommunications network 20.

Please amend the paragraph beginning at page 9, line 11, and continuing to page 9, line 20, as follows:

Some of the embodiments described herein utilize or refer to an ATM end system address (AESA). The concept of ATM end system address is described, e.g., in section 3.0 of *ATM User-Network Interface (UNI) Signaling Specification*, Version 4.0, af-sig-0061.00, July 1996, generated by the ATM Forum Technical Committee, which specifies the use of standard ATM addresses for private and public networks. In general, ~~and an~~ an AESA has an initial domain part (IDP) and a domain specific part (DSP). The initial domain part (IDP) comprises two fields: the authority and format identifier (AFI) and the initial domain identifier (IDI). The domain specific part (DSP) is subdivided into a high order DSP (HO-DSP) and a low order part which consists of the end system identifier (ESI) and a selector (SEL).